ABSTRACT

An MPEG-2 video decoding system simultaneously decodes two or more HD-class MPEG sequences using a single video decoder, and reduces memory capacity and bandwidth. According to the video decoding system, a buffer size is reduced by efficiently sharing a video buffer, and a great reduction of a gate size can be obtained by integrating a VLD unit and a picture controller, and by integrating a motion compensation unit and a memory interface, respectively. Also, two or more HD-class MPEG sequences are displayed in the form of a PIP or a split screen. In the case of the PIP display, a DTV main picture is displayed in a non-compression mode, and a DTV sub-picture is displayed in a 1/4-compression mode. In the case of the split-screen display, the DTV main picture and the DTV sub-picture are displayed in a 1/2-compression mode.